CH7530A DP++ Level Shifter

FEATURES

- Compliant with DisplayPort Dual mode Specification version 1.1
- Output supports up to 300 MHz TMDS clock for video transport with resolution up to 4Kx2K@30Hz or 1920x1080@120Hz
- IIC-over-AUX transaction supported
- DDC buffer and related control register integrated Identifier supported
- Single 3.3V power supply
- 5V power supply output supported with over 50mA current output capability
- Programmable equalizer
- Programmable Pre-Emphasis on output driver supported
- CEC isolation switch supported
- Power saving mode supported
- Low power architecture
- Anti-Back Drive design on sink-side pins
- RoHS compliant and Halogen free package
- HBM 8KV (DP ++ main link pairs pass 5KV)
- Crystal free
- Offered in 40-Pin QFN Package (5 x 5 mm)

GENERAL DESCRIPTIONS

Chrontel's CH7530A is a low-cost, low-power semi-conductor device that translates the DisplayPort dual mode signal to TMDS signal. This innovative device, which integrates programmable equalizer, high speed TMDS level shifter and IIC to AUX translator, is specially designed to target the DP++ adaptor device, docking station and PC market segments.

The CH7530A is compliant with the DisplayPort dual mode standard specification version 1.1. With sophisticated equalizer and high-speed TMDS level shifter integrated, the device's TMDS signal output supports video resolution up to 4Kx2K@30Hz or 1920x1080@120Hz for 3D applications.

The CH7530A also integrates the identifier, IIC over AUX translator and the related DDC control registers, which enables the programmable TMDS output and supports both DDC and AUX signaling on the upstream DisplayPort connector. With step-up regulator integrated, CH7530A supports 5V power supply output.

Application

- DP++ type 2 Cable Adaptor
- Docking Station
- Notebook/Ultrabook/AIO

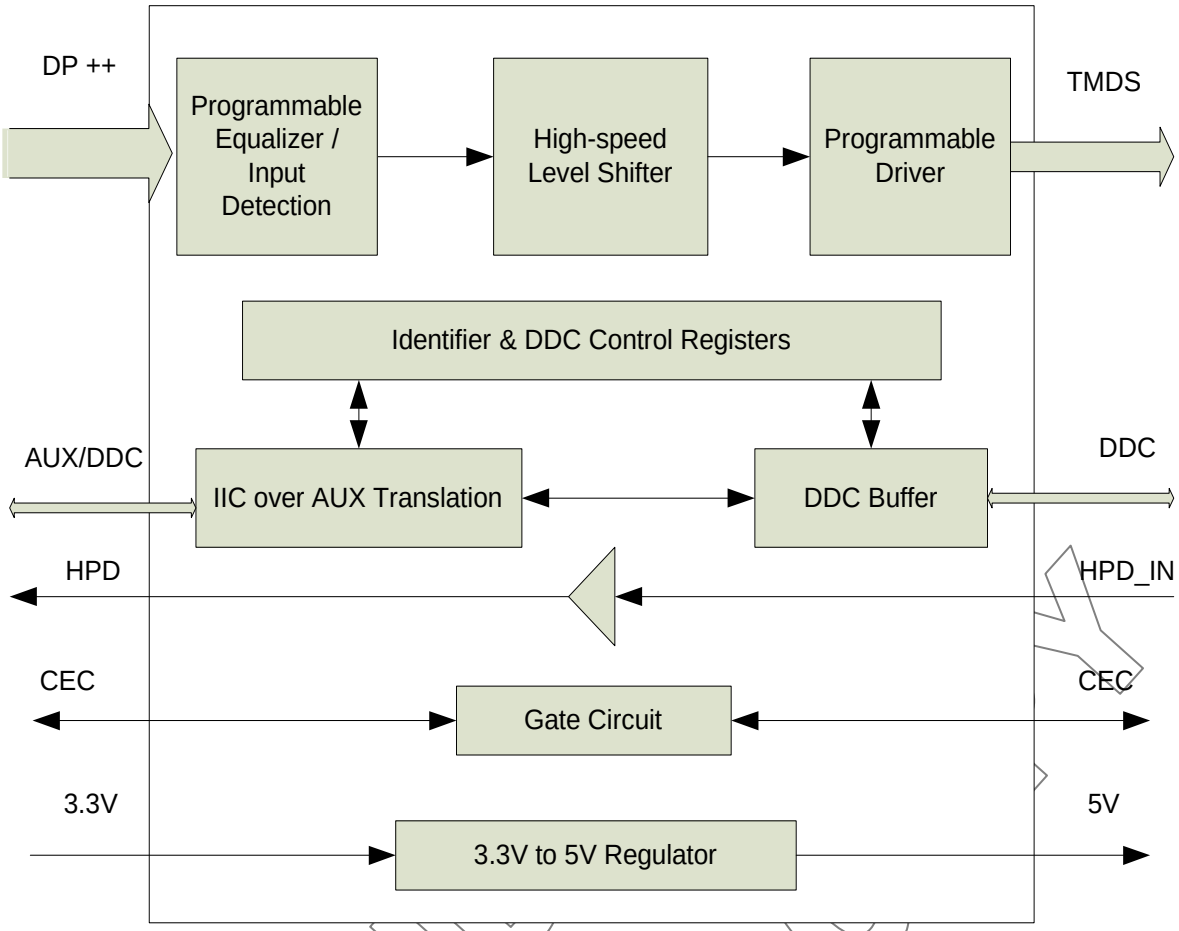

Figure 1: CH7530A Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

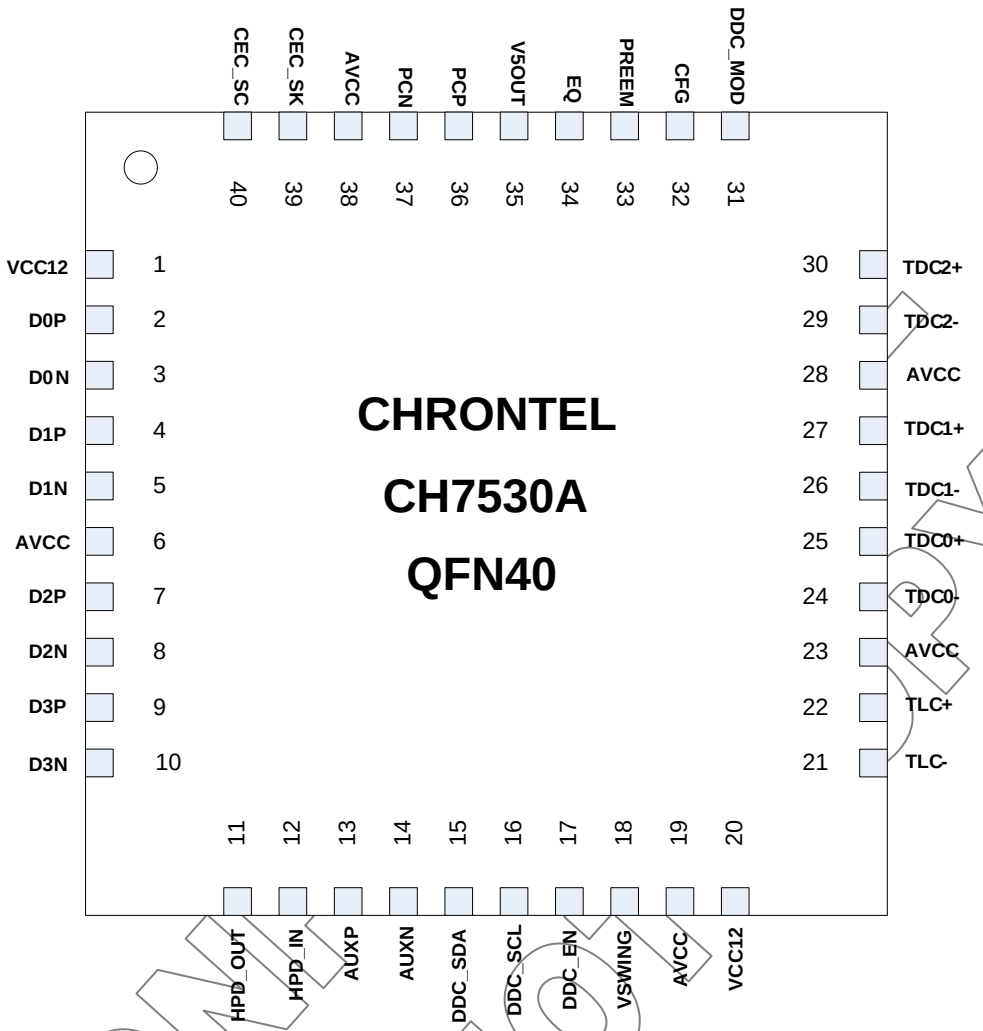

Figure 2: CH7530A 40-Pin QFN Pin Out

1.2 Pin Description

Table 1: CH7530A QFN 40-Pin Descriptions

Pin #	Type	Symbol	Description
2,3,4,5, 7,8,9,10	In	D[3:0]P/N	**DP Dual Mode Main Link Differential Line Input** These pins accept four AC-coupled differential pairs signals from the DisplayPort transmitter.
11	Out	HPD_OUT	**DP Dual Mode Receiver Hot Plug Output**
12	In	HPD_IN	**TMDS Transmitter Hot Plug Input**
13,14	In/Out	AUXP, AUXN	**AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
15	In/Out	DDC_SDA	**Serial Port Data to TMDS Receiver** The pin should be connected to data signal of DDC. This pin requires a pull-up 2 kΩ resistor to the desired voltage level
16	Out	DDC_SCL	**Serial Port Clock Output to TMDS Receiver** The pin should be connected to clock signal of DDC. This pin requires a pull-up 2 kΩ resistor to the desired voltage level
17	In	DDC_EN	**Enables the DDC buffer and level shifter** When DDC_EN = LOW, buffer/level shifter is disabled. When DDC_EN = HIGH, buffer and level shifter are enabled To prevent the back drive from sink via DDC channel. This pin requires a pull-up kΩ resistor to AVCC
18	Out	VSWING	**TMDS Swing Control** This pin sets the swing level of the TMDS outputs. A 11.5kΩ with 1% tolerance resistor should be connected between this pin and TGND using short and wide traces.
21,22	Out	TLC-,TLC+	**TMDS Clock Outputs** These pins provide the differential clock output for the TMDS.
24,25	Out	TDC0-,TDC0+	**TMDS Data Channel 0 Outputs** These pins provide the differential outputs for data channel 0
26,27	Out	TDC1-,TDC1+	**TMDS Data Channel 1 Outputs** These pins provide the differential outputs for data channel 1
29,30	Out	TDC2-,TDC2+	**TMDS Data Channel 2 Outputs** These pins provide the differential outputs for data channel 2
31	In	DDC_MOD	**DDC buffer selection** This pin can be board-strapped to one of four decode values: short to AVCC, 22kΩ resistor to AVCC, open-circuit, 22kΩ resistor to AVSS[1]
32	In	CFG	**TMDS selection**
33	In	PREEM	**Pre-emphasis Setting** This pin can be board-strapped to one of five decode values: short to AVSS, 22kΩ resistor to AVSS, open-circuit, 22kΩ resistor to AVCC, short to AVCC[2]
34	In	EQ	**Programmable Equalizer Setting** Equalizer setting. This pin can be board-strapped to one of five decode values: short to AVSS, 22kΩ resistor to AVSS, open-circuit, 22kΩ resistor to AVCC, short to AVCC[3]
35	Out	V5OUT	**5V Power Supply Output** 5V regulated output from the integrated voltage regulator
36	In	PCP	**Positive terminal for the Power regulator external capacitor**
37	In	PCN	**Negative terminal for the Power regulator external capacitor**
39	In/Out	CEC_SK	**CEC Pin to Sink**

40	In/Out	CEC_SC	**CEC Pin to DP dual mode Source**
1,20	Power	VCC12	**Analog Power Supply (1.2V) with internal LDO**
6,19,23, 28,38	Power	AVCC	**Analog Power Supply (3.3V)**
Therma l Pad	Power	AVSS	**Analog Ground**

Notes:

1. This pin provides DDC buffer configuration, the details are as follow:

Table 2: Pin DDC_MOD Configuration

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k or short to AVSS
DDC buffer	Active buffer	Passive buffer	Active buffer	Passive buffer
PD_LDO	0	0	1	1

2. **Table 3: Driver settings**

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k to AVSS	Short to AVSS
Driver Settings	0dB	3dB	5dB	7dB	10dB

3. **Table 4: Equalizer settings**

Options	Short to AVCC	22k to AVCC	OPEN CIRCUIT	22k to AVSS	Short to AVSS
EQ Settings	1dB	4dB	7dB	10dB	13dB

2.0 PACKAGE DIMENSIONS

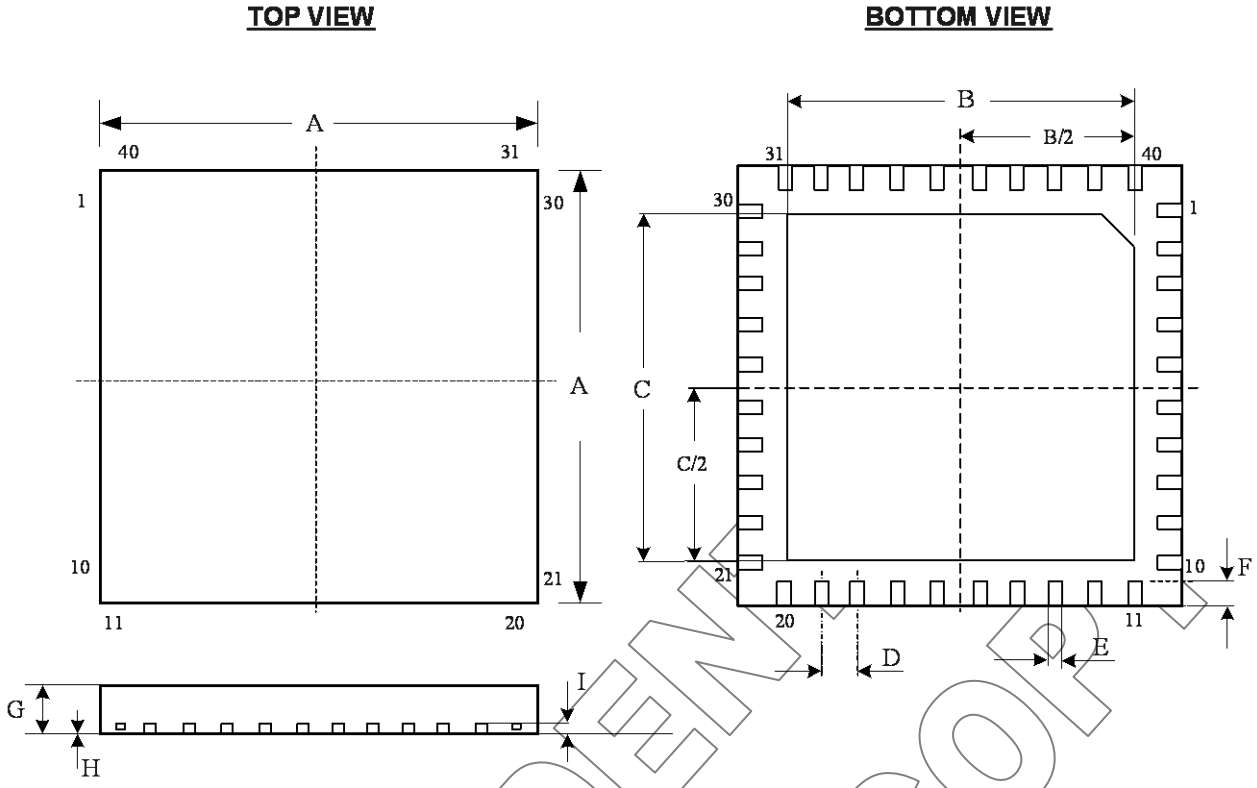

Figure 3: 40 Pin QFN Package

Table 5: Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.70	0	0.203
	MAX	5.10	3.40	3.40		0.25	0.45	0.80	0.05	REF

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7530A-BF	40 QFN, Lead-free	Commercial : 0 to 70°C	490/Tray
CH7530A-BFI	40 QFN, Lead-free	Industrial : -40 to 85°C	490/Tray

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